Keysight Technologies
N4916B De-emphasis Signal Converter

Data Sheet

Version 1.11

Accurately characterize your multi-gigabit serial interfaces with the 4-tap de-emphasis signal converter N4916B with optional clock multiplier

KEYSIGHT TECHNOLOGIES

Introduction

Accurately characterize your multi-gigabit serial interfaces with the 4-tap de-emphasis signal converter N4916B with optional clock multiplier

Key features:

Generates 4-tap de-emphasis with variable de-emphasis levels up to 12.0 dB

-Supports data rates from 660 Mb/s to 14.2 Gb/s
-Tolerates non-balanced patterns
-Transparent to jitter
-Flexible usage as front-end for J-BERT N4903B, ParBERT 81250A or other pattern generators
-Optional clock multiplier (Option 001)
-Small size
-Programmable via J-BERT N4903B or stand-alone

Keysight N4916B Applications

The de-emphasis technique is used in many high-speed serial bus interfaces to compensate for signal distortions caused by the transmission of multi-gigabit electrical signals over PC board traces. With data rates moving beyond 5 Gb/s the simple 2-tap de-emphasis is more and more replaced by 3- or 4-tap de-emphasis techniques, i.e. for front-side buses such as QPI, PCI Express 3.0 or 12G SAS interfaces, or 10GBASE KR backplanes. The Keysight Technologies, Inc. N4916B de-emphasis signal converter enables R&D and test engineers to accurately emulate transmitter de-emphasis with adjustable 4-tap de-emphasis levels, while being transparent to jitter even on non-balanced pattern streams. It can also be used to compensate for distortions caused by cables, fixtures or testboards in the test set up.

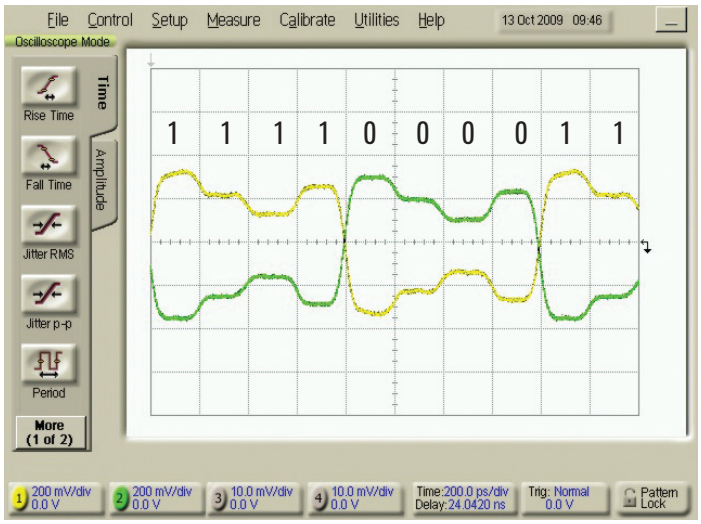


Figure 1. Differential signal with variable de-emphasis on 1 pre-cursor and 2 post-cursors generated by N4916B

The de-emphasis technique is used in many popular gigabit serial bus interfaces operating at data rates above 1 Gb/s, i.e. PCI Express®, USB3, SATA, 10GBASE-KR, 40GBASE-KR4, QPI, memory buses or Infiniband links.

Analyze error, jitter or eye performance of devices using half-rate clocks

Half-rate clocks are used in some of the highest performance serial bus interfaces, such as front-side buses QPI or memory buses.

By using the N4916B's clock multiplier (Option 001), an external clock is provided, to use the analyzer of J-BERT N4903B can be used to accurately characterize the error, eye, jitter performance without using a CDR.

Keysight N4916B Applications

Emulating transmitter de-emphasis

The de-emphasis signal converter N4916B allows emulating a transmitter by varying the de-emphasis in a wide range and for each of the three cursors individually. The N4916B is transparent to jitter on the data and clock signals from the pattern generator. The N4916B outputs are DC coupled, so that even unbalanced pattern streams can be generated without DC drifts.

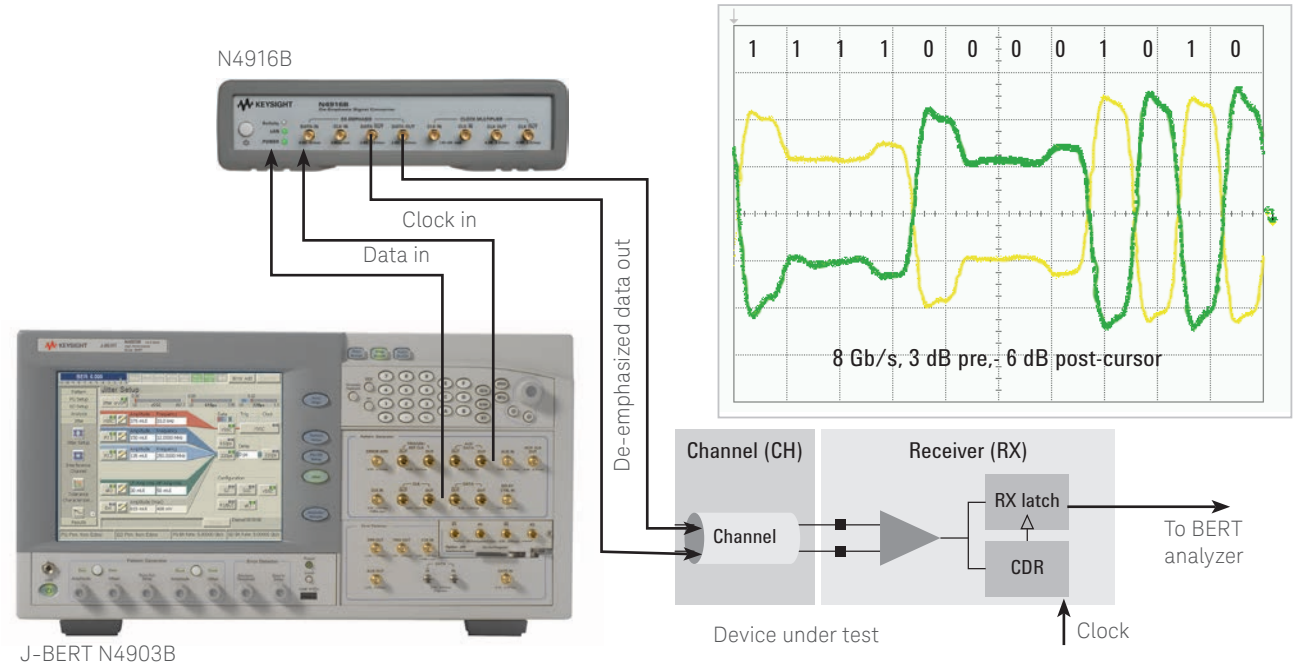


Figure 2. Generating a de-emphasis signal with N4916B and J-BERT N4903B

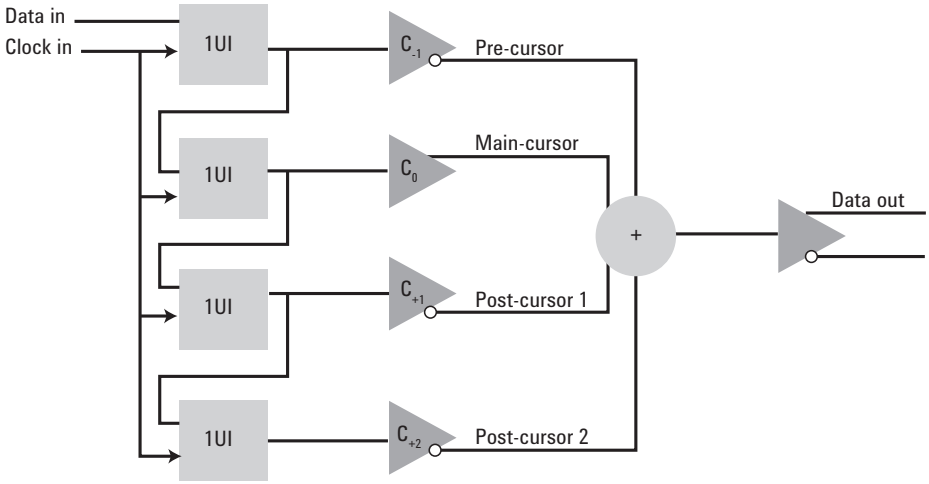
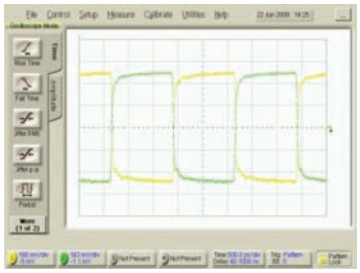


Figure 3. Simplified block diagram of N4916B showing four-tap FIR (finite impulse response) circuit

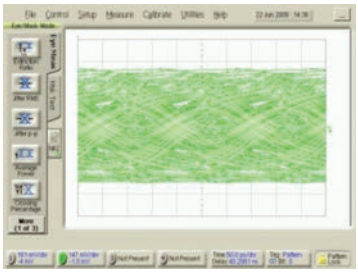
Keysight N4916B Applications

De-embedding signal degradations

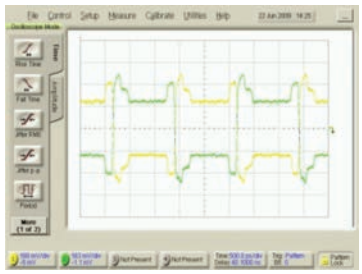
The N4916B can also be used to compensate for some of the signal degradations caused by the test set up; e.g. cables, fixtures, test boards. This is helpful to optimize the jitter budget needed for accurate receiver tolerance characterization.



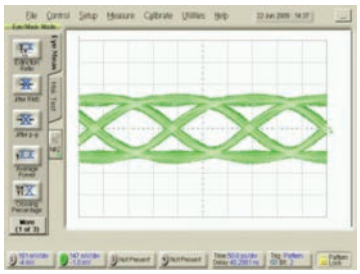
No TX de-emphasis



Closed eye at receiver input



With TX de-emphasis



Open eye at receiver input

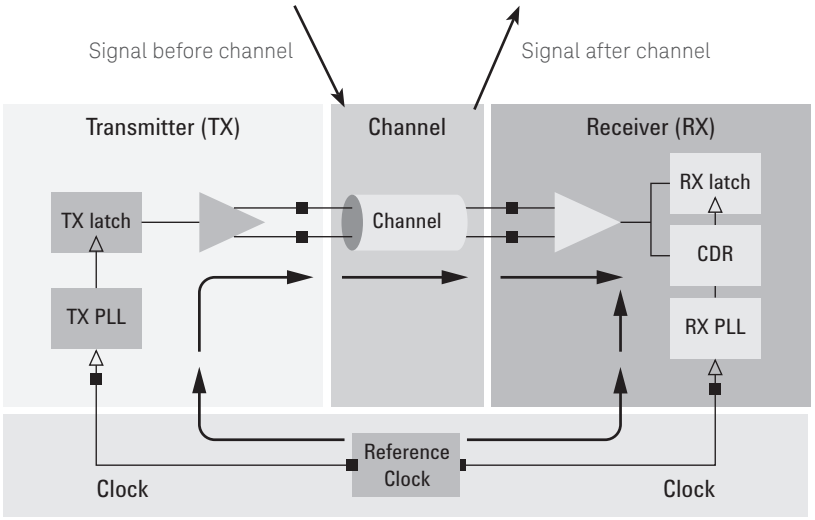


Figure 4. De-emphasis helps to compensate for the signal degradations caused by the channel. Also some of the signal degradations caused by cables, fixtures or test boards in the test setup can be compensated for using de-emphasis.

Keysight N4916B Applications

Analyze BER and eye performance of half-rate clocked devices

The clock multiplier option enables BER measurements using the forwarded half-rate clock to be used as sampling clock for J-BERT N4903B.

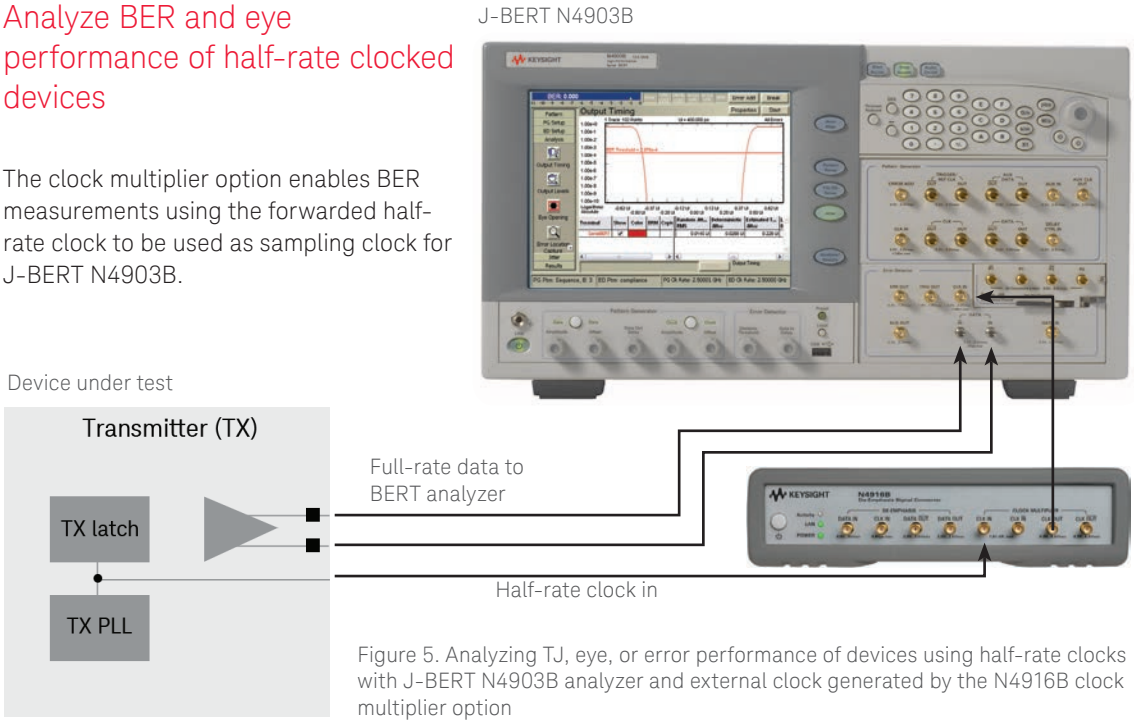


Figure 5. Analyzing TJ, eye, or error performance of devices using half-rate clocks with J-BERT N4903B analyzer and external clock generated by the N4916B clock multiplier option

Control and programming

The N4916B can be controlled via USB interface from the J-BERT N4903B user interface or from a stand-alone user interface.Programming examples are provided.

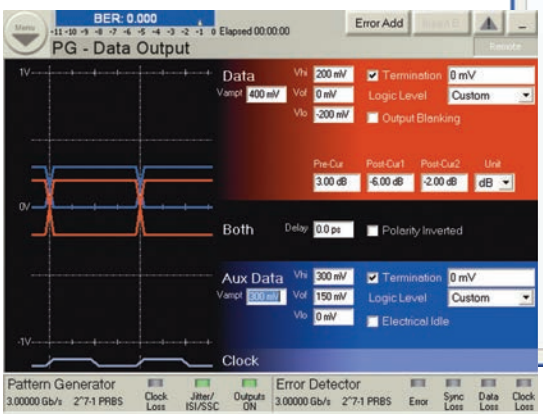


Figure 6. Convenient control of de-emphasis parameters via the GUI of J-BERT N4903B

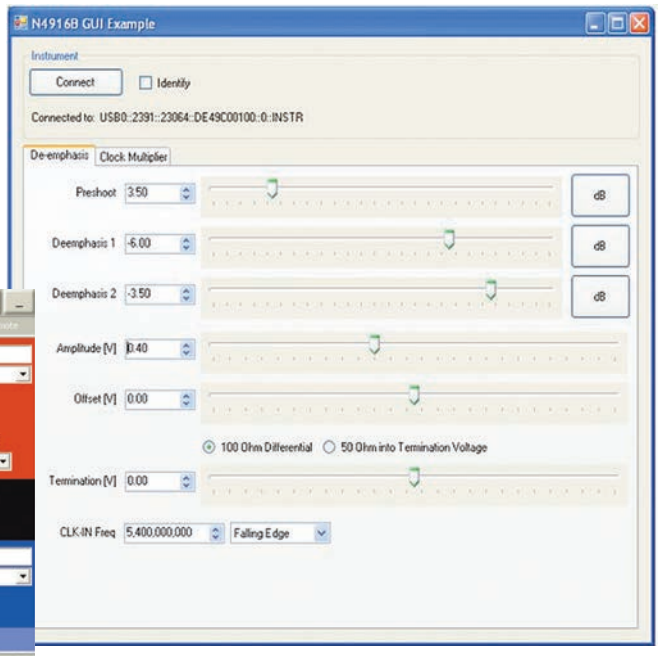


Figure 7. The N4916B can be controlled from a PC program, when operating as front-end for ParBERT 81250A or J-BERT N4903A or other pattern generators.

Keysight N4916B Specifications

De-emphasis signal converter	
Data rate	660 Mb/s to 14.2 Gb/s
Output format	NRZ
Pre-cursor	0 to +12.0 dB/0.1 dB resolution [2]
Post-cursor 1	0 to –12.0 dB/0.1 dB resolution [2]
Post-cursor 2	0 to –8.0 dB/0.1 dB resolution [2]
Cursor accuracy	± 1.0 dB typical at PCI Express 3.0 pre-sets for 8 Gb/s
Clock input, data input	50 Ω single ended, DC coupled
De-emphasis output	50 Ω differential, DC coupled. Terminate unused output.
Output amplitude	100 mV to 800 mV single ended, 200 mV to 1600 mV differential
Output voltage window	± 2 V
Coupling	DC, accepts unbalanced patterns
External termination voltage	± 2 V
Output transition times	< 30 ps typical (20% - 80%)
Jitter added	< 300 fs rms typical (0101 pattern)
Jitter transfer	Transparent to clock jitter. Data and clock must carry the same amount of jitter and need to be in phase [1]
Delay added	1.5 UI + 920 ps typical (including input and output adapters and ideal clocking at 0.5 UI)
Input voltage data input	1.26 Vpp, offset –0.79 V
Input voltage clock input	0.3 Vpp, offset 0 V
Connectors	SMA female

1. We recommend use of J-BERT N4903B's Aux clock output to ensure these prerequisites are met. When using N4916B together with J-BERT N4903A or ParBERT, jitter injection might be limited.
2. Polarity as depicted. Sum of all cursors cannot exceed maximum voltage output swing and window. The N4916B voltage amplitude Vpp is defined as the maximum positive sum of all cursors (Vd) = |Pre Amplitude| + |Main Amplitude| + |Post1 Amplitude| + |Post2 Amplitude|; this is in reference to the PCI Express 3.0 specification as shown in Figure 8

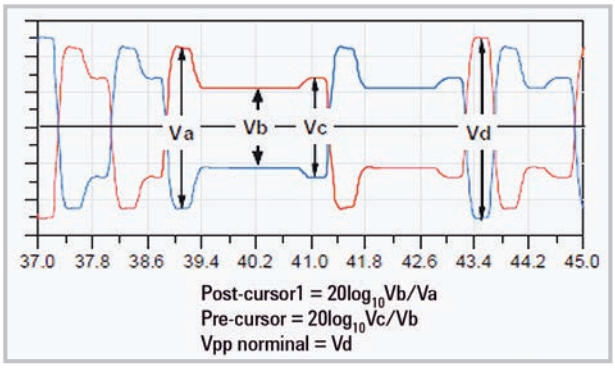


Figure 8. Definition of nominal output amplitude and de-emphasis amplitude

Figure 9. Front panel view of N4916B

Keysight N4916B Specifications (continued)

Clock multiplier	
Input frequency range	1 to 7.5 GHz, Duty cycle 45-55%
Multiplier factors	1, 2
Input	50 Ω single ended, AC coupled
Input voltage swing	100 mV to 1 V differential
Input termination voltage	± 2 V
Output	50 Ω differential, replace by: AC coupled. Terminate unused output
Output voltage swing	> 500 mV differential
Output transition time	< 30 ps typical (20% – 80%)
Jitter added	< 500 fs rms typical
Connector	SMA female
General characteristics	
Operating temperature	5 °C to 40°C (–23 °F to 104 °F)
Storage temperature	–40 °C to +70°C (–65 °F to 158 °F)
Operating Humidity	95% relative humidity, non-condensing
Storage humidity	50 % relative humidity
Power requirements	100 V to 240 V, 47 Hz to 63 Hz, 80 VA, the maximum allowed voltage fluctuation is 10%
Physical dimensions WxHxD	Bench top (with bumper) 228 x 59 x 246 mm Rack mount (without bumper) 1/2* 19" width, 1U height: 213 x 44.5 x 245 mm
Weight net	2.05 kg (4.51 lb)
Weight shipping	4.65 kg (10.25 lb)
Recommended recalibration period	1 year recommended
Warranty period	3 years return to Keysight. See ordering instructions for extended warranty

Figure 10. Rear panel view of N4916B

Keysight N4916B Specifications (continued)

Regulatory standards	
Safety	IEC61010-1:2001, EN61010-1:2001, CAN/CSA-C22 No. 61010-04, UL 61010-1:2004
EMC	IEC61326-1:1997+A1:1998, EN61326-1:1997+A1:1998
Quality management	ISO 9004, ISO 14000
Remote control interfaces	
Connectivity	USB 2.0, rear panel, LAN
Programming language	SCPI
Via J-BERT	Via USB 2.0 to the controlling J-BERT N4903B, which provides LAN, GPIB, USB as remote control interfaces. The N4903B requires software revision 6.5x or higher to control the N4916B; to control the 14.2 Gb/s version of N4916B (serial numbers MY51300500 and higher), the J-BERT N4903B software revision 7.0 is needed
Stand-alone user interface	
System requirements	OS: Microsoft Windows (verified on XP, SP2), Keysight I/O Libraries Suite rev.15.5, Microsoft .NET 2.0

Specification assumptions

The specifications in this document describe the instruments warranted performance. Preliminary values are shown in italic. Non-warranted values are described as typical. All specifications are valid in a range from 5 °C to 40 °C ambient temperature after a warm-up time of 30 minutes and after manual calibration of input clock and data timing. If not otherwise stated, all inputs and outputs need to be terminated with 50 Ω to GND.

Ordering Information

Accessories included in N4916B	**4 x 50 Ω terminations 3.5 mm, USB cable, test report "UK6", CD-ROM with software and user documentation**
4-tap de-emphasis signal converter	N4916B-STD
Clock multiplier	N4916B-001
Recommended accessories	
Matched cable pair for connecting data and clock input to J-BERT N4903B	N4915A-010
Adapter 3.5 mm (f) to 2.4 mm (m) (1 each is needed for connecting N4916B with N4915A-010 cable kit to N4903A or ParBERT)	N4911A-002
Rack mount kit	E5810A-100
Warranty and calibration services	
Warranty and calibration services	R1280, R1282
Productivity assistance	R1380-N49xx

Related Keysight Literature

Remote control interfaces	
J-BERT N4903B High-Performance Serial BERT Data Sheet	5990-3217EN
81250A ParBERT Data Sheet	5968-9188EN
De-emphasized signal generation with N4916A Application Note	5989-7193EN

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