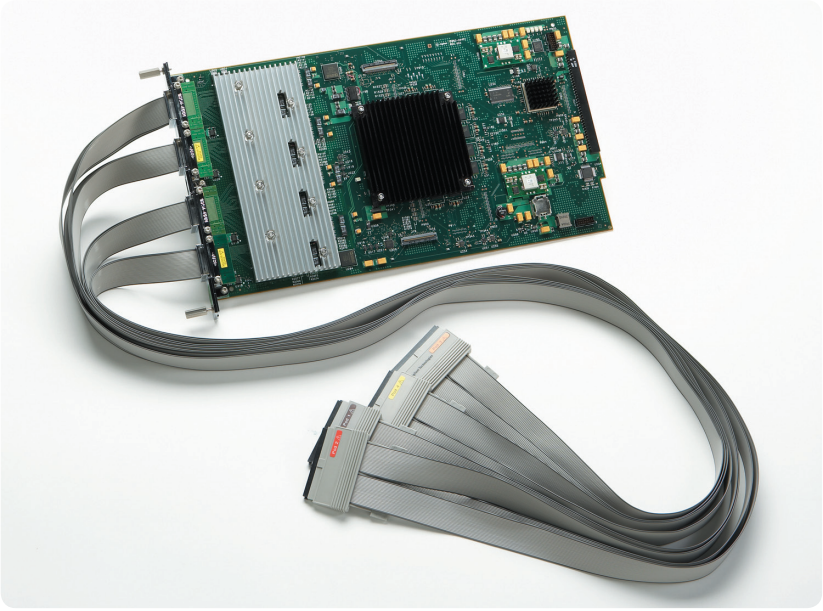
Agilent 16962A 2 GHz State, 2/4/8 GHz Timing Logic Analyzer Module

Data Sheet



Features:

- State analysis up to 2 GHz and dual state analysis up to 2.5 Gb/s addresses all DDR speeds
- Up to 125 ps (8 GHz) timing analysis captures up to 400 M of system activity at high resolution
- 68-channel cards combined in up to 5-card sets provide 340 channels on a single time base and trigger
- Selectable memory depths up to 100 M enables you to purchase the memory depth you need now and upgrade later as your needs evolve

The Agilent 16962A logic analyzer module delivers the performance required for the latest high-speed standards and devices like DDR3 and A/D converters. In addition to covering emerging standards, the 16962A provides conventional state and timing measurements on single-ended or differential signals at rates up to 2 GHz. The 100 M samples of memory ensure you capture enough system activity to troubleshoot complex systems.

Optimized for comprehensive DDR memory analysis

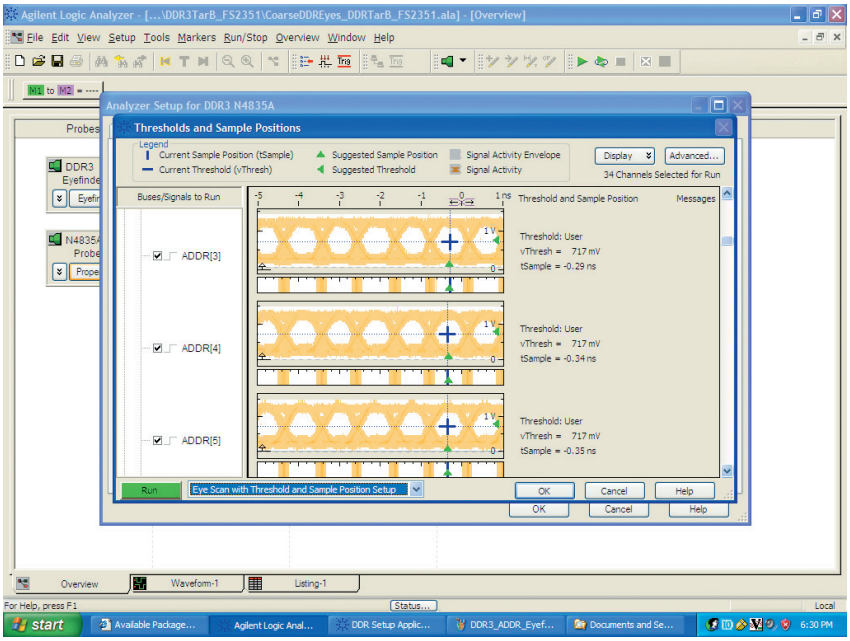
The 16962A logic analysis module with 2.0 GT/s state speed and 2 GHz trigger sequencer speed provides full capability to reliably trigger and capture all DDR activity, including DDR3 2133. When used with a full suite of DDR probing solutions (Interposer, BGA, SODIMM, mid-bus) and compliance/performance analysis software, you obtain full test capability for system integration in the memory industry.

Automate measurement setup and quickly gain diagnostic clues

Quickly get up and running by automating your measurement setup process. In addition, the logic analyzer's sampling position and threshold voltage settings are automatically determined so that data on high-speed buses is captured with the highest accuracy.

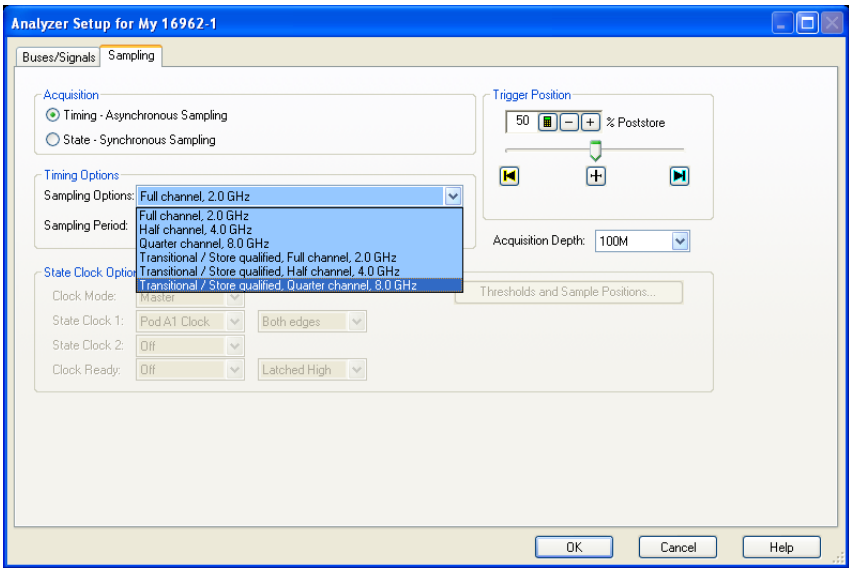
Identify problem signals over hundreds of channels simultaneously

As timing and voltage margins continue to shrink, confidence in signal integrity becomes an increasingly vital requirement in the design validation process. Eye scan lets you acquire signal integrity information on all the buses in your design, under a wide variety of operating conditions, in a matter of minutes. Identify problem signals quickly for further investigation with an oscilloscope. Results can be viewed for each individual signal or as a composite of multiple signals or buses.



Maximize the amount of time captured at high-speed resolution

In timing mode you typically have to sacrifice sampling resolution to acquire more system activity. If your system has bursts of activity followed by times with little activity, you can use transitional timing along with the logic analyzer's deep memory to capture seconds to minutes of activity at 125 ps (8 GHz) sampling resolution. You also have the flexibility to increase the amount of time captured by excluding certain buses or signals from being stored like clock or strobe signals that add little useful information to the measurement.



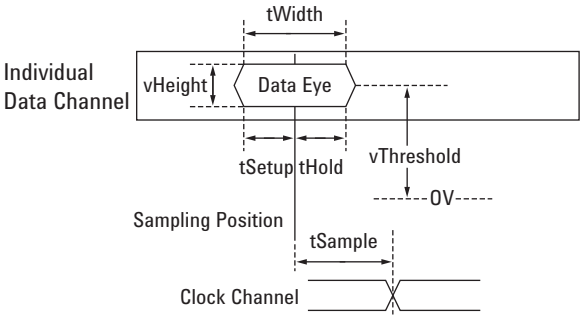
16962A Key Specifications and Characteristics

Agilent model number	16962A		
Channels per card (unused clock and clock ready bits can be used as data bits)	68 channels State: 64 data + 2 clock + 2 clock ready Timing: 68 data channels		
Maximum channels on single time base and trigger	340 channels		
Number of mainframe slots per card	1		
Number of independent analyzers per module set	1		
Timing modes – Conventional and transitional	**Quarter channel mode**	**Half channel mode**	**Full channel mode**
Maximum sample rate	125 ps (8 GHz)	250 ps (4 GHz)	500 ps (2 GHz)
Maximum memory depth *	(4x memory option)	(2x memory option)	
Option 100	400 M	200 M	100 M
Option 064	256 M	128 M	64 M
Option 032	128 M	64 M	32 M
Option 016	64 M	32 M	16 M
Option 004 (included standard)	16 M	8 M	4 M
Channels per multi-card module			
1-card module	17	34	68
2-card module	34	68	136
3-card module	51	102	204
4-card module	68	136	272
5-card module	85	170	340
Minimum data pulse width	400 ps	400 ps	1 sample period + 150 ps
Time interval accuracy	± (1 sample period + 400 ps + 0.01% of time interval reading)		
Pod usage	1 pod from each pod pair, user selectable	1 pod from each pod pair, user selectable	All pods
Channel usage	Even bits of selected pods	All channels of selected pods	All channels
Probe connection	E5386A adapter recommended between probe and logic analyzer cable for selected pods	Direct to logic analyzer cable for selected pods	Direct to logic analyzer cable

* *In transitional timing mode, the number of transitions stored will be between half of the maximum memory depth and up to the maximum memory depth depending on the rate at which the signals transition.*

16962A Key Specifications and Characteristics (continued)

Agilent model number	16962A
State modes	
Maximum state speed [1]	2 GHz (single edge, 2 GHz clock)
Maximum dual sample state rate	2.5 Gb/s
Minimum state speed	40 MHz (single edge) 20 MHz (both edge)
Maximum state data rate *,1	2 Gb/s (DDR, 1 GHz clock)
Channels per multi-card module	State
1-card module	64 data + 2 clocks + 2 clock ready
2-card module	132 data + 2 clocks + 2 clock ready
3-card module	200 data + 2 clocks + 2 clock ready
4-card module	268 data + 2 clocks + 2 clock ready
5-card module	336 data + 2 clocks + 2 clock ready
Maximum memory depth	
Option 100	100 M
Option 064	64 M
Option 032	32 M
Option 016	16 M
Option 004 (included standard)	4 M
Minimum time between active clock edges	500 ps
Maximum time between active clock edges	25 ns
Minimum state clock pulse width [2]	
Single edge	250 ps
Multiple edge	500 ps
Number of clocks	2 (on odd pods), 1 can be selected
Number of clock ready inputs	2 (on even pods), 1 can be selected
Time tag resolution	25 ps
Clock qualifier setup time	300 ps
Clock qualifier hold time	0 ps
Maximum time count between stored states	83.4 days
Automated threshold/sample position, Simultaneous eye diagrams, all channels	Yes
Data valid window	
tWidth	200 ps typical
tSetup	.5tWidth
tHold	.5tWidth
tSample adjustment resolution	5 ps
tSample accuracy, manual adjustment	± 150 ps
vHeight	200 mV



* *Items marked with an asterisk (*) are specifications. All others are characteristics. "Typical" represents the average or median value of the parameter based on measurements from a significant number of units.*

1. *Requires continuous, periodic clock.*
2. *Tested with input signal Vih = 1.125 V, Vil = 0.875 V, threshold = 1.0 V, tr/tf = 180 ps ±30 ps (10%, 90%).*

16962A Key Specifications and Characteristics (continued)

Agilent model number	16962A	
Maximum memory depth [1]		
	State	**Timing (full/half/quarter ch)**
Option 100	100 M	100 M/200 M/400 M
Option 064	64 M	64 M/128 M/256 M
Option 032	32 M	32 M/64 M/128 M
Option 016	16 M	16 M/32 M/64 M
Option 004 (included standard)	4 M	4 M/8 M/16 M
Memory depth upgrade after purchase	Available via E5887A	
Trigger characteristics		
Maximum trigger sequencer speed	2 GHz (500 ps)	
Trigger resources – create a trigger from any 8 of the listed resources (7 in transitional timing)	16 pattern detectors evaluated as =, !=, >, ≥, <, ≤, in range, not in range 8 range detectors 4 to 8 burst detectors 4 edge detectors in timing, 3 in transitional timing 4 flags 1 timer in timing or transitional timing 1 arm in	
Trigger resource combinations	Arbitrary Boolean combinations	
Trigger actions	Goto Trigger and fill memory Trigger and Goto Trigger, send e-mail, and fill memory	
Store qualification actions (available in state mode)	Store sample Don't store sample Turn on default storage Turn off default storage Store sample and turn on default storage Don't store sample and turn off default storage	
Timer actions	Start from reset Stop and reset Pause Resume	
Flag actions	Set Clear Pulse set Pulse clear	
Maximum trigger sequence levels	4	
Trigger sequence level branching	Arbitrary 4-way if/then/else	
Trigger position	Start, center, end, or user-defined	
Maximum pattern width	128 bit – single label 340 bit – AND of multiple labels across multi-card set	
Other		
Supported signal types	Single-ended and differential	
Probe compatibility	90-pin cable connector	
Voltage threshold	–3 V to 5 V in 10 mv increments	
Threshold accuracy	± (30 mV + 1% of setting)	
Threshold setting granularity	By channel	

1. Store qualification consumes 1 sample per store qualified block.

16962A Key Specifications and Characteristics (continued)

16962A	
Logic analyzer mainframe compatibility	
16901A 2-slot modular logic analysis system 16902B 6-slot modular logic analysis system (Requires software revision 3.83 or greater)	
Power requirements	
All necessary power is supplied by the backplane connector of the logic analyzer mainframe.	
Environmental characteristics	
Indoor use only	
Operating environment	
Temperature	0 °C to 40 °C (+32 °F to 104 °F). Reliability is enhanced when operating within the range +20 °C to +35 °C (+68 °F to +95 °F)
Humidity	0 to 80% relative humidity at 40 °C (+104 °F). Reliability is enhanced when operating within the range 20% to 80% non-condensing
Altitude	0 to 3,000 m (10,000 ft)
Vibration	Random vibration 5 to 500 Hz, 10 minutes per axis, approximately 0.2 g rms
Non-operating environment	
Temperature	–40 to +75 °C (–40 to +167 °F). Protect the instrument from temperature extremes which cause condensation on the instrument.
Humidity	0 to 90% at 65 °C (149 °F)
Altitude	0 to 15,300 m (50,000 ft)
Vibration (in shipping carton)	Random vibration 5 to 500 Hz, 10 minutes per axis, approximately 2.41 g rms; and swept sine resonant search, 5 to 500 Hz, 0.50 g (0-peak), 5 minute resonant dwell at 4 resonances per axis.

Ordering Information

16962A 2/4/8 GHz timing, 2 GHz state logic analyzer

Base configuration: 4 M acquisition memory included standard

- Option 016 – increase acquisition memory to 16 M
- Option 032 – increase acquisition memory to 32 M
- Option 064 – increase acquisition memory to 64 M
- Option 100 – increase acquisition memory to 100 M

E5887A after-purchase, memory upgrade for 16962A logic analyzer modules

Upgrade your 16962A logic analyzer module by "turning on" additional memory depth when you need more. Purchase the capability you need now, then upgrade as your needs evolve.

- Option 016 – increase acquisition memory to 16 M
- Option 032 – increase acquisition memory to 32 M
- Option 064 – increase acquisition memory to 64 M
- Option 100 – increase acquisition memory to 100 M

Agilent DDR memory probes and analysis software

The following DDR probing and DDR decoder/analysis products are available from Agilent. To ensure a complete solution that is compatible with your specific DDR application and measurement needs, please contact Agilent or Agilent's third party vendors. For DDR3 2133, contact Agilent for configuration considerations.

Product	Description
DDR2 BGA probes	
W2631B	DDR2 x16 BGA command and data probe for logic analyzer and oscilloscope – kit of 4 probes
W2632A	DDR2 x16 BGA data probe for logic analyzer and oscilloscope – kit of 4 probes
W2633B	DDR2 x8 BGA command and data probe for logic analyzer and oscilloscope – kit of 4 probes
W2634A	DDR2 x8 BGA data probe for logic analyzer and oscilloscope – kit of 4 probes
ZIF probes (used to connect W2630A/B Series DD2 BGA probes to 90-pin logic analyzer cables)	
E5384A	46-ch single-ended ZIF probe for x8/x16 DRAM BGA probe connection to 90-pin logic analyzer cable
E5826A	46-ch single-ended ZIF probe for x16 DRAM data only BGA probe connection to 90-pin logic analyzer cable
E5827A	46-ch single-ended ZIF probe for 2 x8 DRAMs data only BGA probe connection to 90-pin logic analyzer cable
DDR3 BGA probes	
W3631A-001	Quantity of 1 – DDR3 x16 BGA command and data probe for logic analyzers and oscilloscopes
W3631A-002	Quantity of 2 – DDR3 x16 BGA command and data probe for logic analyzers and oscilloscopes
W3631A-004	Quantity of 4 – DDR3 x16 BGA command and data probe for logic analyzers and oscilloscopes
W3633A-001	Quantity of 1 – DDR3 x4/x8 BGA command and data probe for logic analyzers and oscilloscopes
W3633A-002	Quantity of 2 – DDR3 x4/x8 BGA command and data probe for logic analyzers and oscilloscopes
W3633A-004	Quantity of 4 – DDR3 x4/x8 BGA command and data probe for logic analyzers and oscilloscopes
ZIF probes (used to connect W3630A Series DD3 BGA probes to 90-pin logic analyzer cables)	
E5845A	46-ch SE ZIF probe for DDR3 x16 DRAM BGA probe connection to 90-pin logic analyzer cable
E5847A	46-ch SE ZIF probe for DDR3 x4/x8 DRAM BGA probe connection to 90-pin logic analyzer cable
DDR2/3 and LPDDR/LPDDR2 analysis software	
B4621B	DDR2/3/4 bus decoder
B4622B	DDR2/3/4 and LPDDR/LPDDR2 protocol compliance and analysis tool
B4623B	LPDDR/2/3 bus decoder

Ordering Information (continued)

Third party DDR memory probes and analysis software

The following DDR components are available from Agilent's third party partners:

- For DDR1 DIMM Interposers contact FuturePlus Systems at **http://www.futureplus.com/agilent**
- For DDR2 DIMM or SODIMM Interposers contact FuturePlus Systems at **http://www.futureplus.com/agilent**
- For DDR3 DIMM or SODIMM Interposers contact either FuturePlus Systems at **http://www.futureplus.com/agilent** or Nexus Technologies at **http://www.nexustesttechnology.com**

General purpose logic analyzer probes

Probes are ordered separately. Please specify probes when ordering to ensure the correct connection between your logic analyzer and device under test.

The following probes are compatible with the 90-pin cable of the 16962A logic analyzer module.

Probe type	Model number	Channels	Maximum data rate	Supported signal types
Soft touch connectorless probes	E5406A (Pro series)	34 (32 data, 2 clock)	> 2.5 Gb/s	Single-ended data, differential or single-ended clock
	E5402A (Low profile)	34 (32 data, 2 clock)	> 2.5 Gb/s	Single-ended data, differential or single-ended clock
	E5390A (Classic)	34 (32 data, 2 clock)	> 2.5 Gb/s	Single-ended data, differential or single-ended clock
	E5398A (Half-size)	17 (16 data, 1 clock)	> 2.5 Gb/s	Single-ended data, differential or single-ended clock
	E5405A (Pro series)	17 (16 data, 1 clock)	> 2.5 Gb/s	Differential or single-ended data, differential or single-ended clock
	E5387A (Classic)	17 (16 data, 1 clock)	> 2.5 Gb/s	Differential or single-ended data, differential or single-ended clock
Samtec connector probes	E5378A	34 (32 data, 2 clock)	1.5 Gb/s	Single-ended data, Differential or single-ended clock
	E5379A	17 (16 data, 1 clock)	1.5 Gb/s	Differential or single-ended data, Differential or single-ended clock
Mictor connector probe	E5380A	34 (32 data, 2 clock)	600 Mb/s	Single-ended data, Differential or single-ended clock
General purpose flying lead probes	E5382A	17 (16 data, 1 clock)	1.5 Gb/s	Single-ended data, Differential or single-ended clock
	E5381A	17 (16 data, 1 clock)	1.5 Gb/s	Differential or single-ended data, Differential or single-ended clock

Ordering Information (continued)

E5386A adapter and 16962A module quantity requirements

When operating in 8 GHz quarter channel timing mode, the E5386A adapter enables easy signal connection and reduces the number of probes and connectors used in quarter channel timing mode. The adapter maps the appropriate logic analyzer channels to all pins of the probe to which it is connected.

Use the E5386A adapter when operating the 16962A in quarter channel timing modes

Probe models	Number of channels	Quantity of E5386A	Quantity of 16962A
E5379A, E5387A, E5398A, E5405A	17	1	1
E5378A, E5380A, E5390A, E5402A, E5406A	34	2	2
E5384A, E5826A, E5827A, E5845A, E5847A	46	3	3

Related Agilent Literature

Publication title	Pub number
Agilent 16900 Series Logic Analysis System Mainframes - Data Sheet	5989-0421EN
W2630A Series DDR2 BGA Probes for Logic Analyzers and Oscilloscopes - Data Sheet	5989-5964EN
W3630A Series DDR3 BGA Probe for Logic Analyzers and Oscilloscopes - Data Sheet	5990-3179EN
B4621B for DDR2, DDR3, or DDR4 Debug and Validation - Data Sheet	5991-0802EN
B4622B DDR2/3 Protocol Compliance and Analysis Tool - Data Sheet	5991-1063EN
B4623B Bus Decoder for LPDDR, LPDDR2, or LPDDR3 Debug and Validation - Data Sheet	5991-1064EN

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